--21. A semiconductor device comprising:

a gate member over a semiconductor;

source and drain regions in the semiconductor, one of said source and drain regions having a depth not deeper than 0.1μm;

a channel region interposed between said source and drain regions, said channel region having a length not longer than 1μm,

wherein said source and drain regions extends from a surface of said semiconductor to said depth not longer than a thickness of said semiconductor.

~~22~~. A semiconductor device according to claim ~~21~~ wherein said length of the channel region is not longer than 0.3μm.

~~23~~. A semiconductor device according to claim ~~21~~ wherein said semiconductor is a crystal silicon.

24. A memory comprising:

a gate electrode having a floating gate, a control gate and an oxide over a semiconductor substrate, said oxide being provided on surfaces of the floating gate and the control gate;

source and drain region in the semiconductor, one of said source and drain regions having a depth not deeper than 0.1μm;

a channel region interposed between said source and drain regions, said channel region having a length not longer than 1μm,

wherein an edge of said one of the source and drain regions is coincide with

that of said gate electrode, and

wherein the other one of said source and drain regions overlaps with said gate electrode.

25. A semiconductor device according to claim 24 wherein said length of the channel region is not longer than 0.3μm.

26. A semiconductor device according to claim 24 wherein said semiconductor substrate is a crystal silicon substrate.

27. A semiconductor device according to claim 24 wherein said floating gate is formed on the other one of said source and drain regions while said floating gate is not formed on said one of the source and drain regions.

28. A semiconductor device comprising:

a gate member over a semiconductor substrate;

a gate insulator interposed between the gate member and the semiconductor substrate;

a pair of shallower impurity regions in adjacent with said gate member;

a pair of deeper impurity regions in adjacent with said shallower impurity region;

a channel region interposed between said pair of the shallower impurity regions,

wherein said channel region has a length not longer than 1μm, and

wherein said shallower impurity region has a depth not deeper than 0.1μm.

29. A semiconductor device according to claim 28 wherein said length of the channel region is not longer than 0.3μm.

30. A semiconductor device according to claim 28 wherein said semiconductor substrate is a crystal silicon substrate.

31. A semiconductor device according to claim 28 wherein side walls are formed on the pair of said shallower impurity regions.

32. A semiconductor device according to claim 28 wherein the pair of said shallower impurity regions are lightly doped drain regions.

B1 33. A semiconductor device comprising:

a semiconductor substrate;

a first silicon film introduced with an n-type impurity over said semiconductor substrate;

a second film introduced with an n-type impurity over said first silicon film;

an insulating film interposed between said semiconductor substrate and said first silicon film and between said first and second silicon film;

a first impurity region formed in the semiconductor substrate, said first impurity region overlapping with said insulating film;

a second impurity region formed in the semiconductor substrate, second impurity region being not contact with said first impurity region and having a depth not deeper than 0.1μm;

a channel region formed between said first and second impurity region, said channel region having a length not longer than 1μm.

34. A semiconductor device according to claim 33 wherein said length of the channel region is not longer than 0.3μm.

35. A semiconductor device according to claim 33 wherein said semiconductor substrate is a crystal silicon substrate.

36. A semiconductor device according to claim 33 wherein a floating gate is formed on said first impurity region while said floating gate is not formed on said second impurity region.

37. A semiconductor device comprising:

a semiconductor substrate;

at least two gate electrodes over said semiconductor substrate;

a first impurity region formed between said gate electrodes;

at least two second impurity regions formed in adjacent with said gate electrodes, each of said second impurity region having a depth shallower than that of said first impurity region;

at least two channel regions in the semiconductor substrate, each of said channel regions being formed between said first impurity region and each of second impurity regions,

wherein each of said channel regions has a length not longer than 1μm,

wherein said depth of each of said second impurity regions is not deeper than 0.1μm.

38. A semiconductor device according to claim 37 wherein said length of the channel region is not longer than 0.3μm.

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~~39.~~ A semiconductor device according to claim ~~37~~ wherein said semiconductor substrate is a crystal silicon substrate.

Sub C6 40. A semiconductor device according to claim 37 wherein a floating gate is formed on said first impurity region while said floating gate is not formed on each of said second impurity regions.

41. A semiconductor device comprising:

a semiconductor substrate;

at least two gate electrodes over said semiconductor substrate, each of said gate electrodes having a floating gate, a control gate and an oxide on said semiconductor substrate, said oxide being provided on surfaces of the floating gate and the control gate;

a first impurity region formed between said gate electrodes;

at least two second impurity regions formed in adjacent with said gate electrodes, each of said second impurity region having a depth shallower than that of said first impurity region;

at least two channel regions in the semiconductor substrate, each of said channel regions being formed between said first impurity region and each of second impurity regions,

wherein each of said channel regions has a length not longer than 1μm,

wherein said depth of each of said second impurity regions is not deeper than 0.1μm.

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~~42.~~ A semiconductor device according to claim ~~41~~ wherein said length of the channel region is not longer than 0.3μm.